Product Specification

Part Name	:	OEL Display Module
Customer Part ID	:	
WiseChip Part ID	:	UC-1602ASWEG01
Doc No.	:	SAS1-0V016-B

Customer:

Approved by

From: WiseChip Semiconductor Inc.

Approved by

WiseChip Semiconductor Inc.
8, Kebei RD 2, Science Park, Chu-Nan, Taiwan 350, R.O.C.

Notes:

1. Please contact WiseChip Semiconductor Inc. before assigning your product based on this module specification
2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by WiseChip Semiconductor Inc. for any intellectual property claims or other problems that may result from application based on the module described herein.

Revised History

Part Number	Revision	Revision Content	Revised on
UC-1602ASWEG01	A	New	November 19, 2012
UC-1602ASWEG01	B	Page 1 Section 1.2 Add Module size Add Panel size remark Add weight tolerance Page 9~13 Section 3.3 Revised AC characteristics Page 15&17 Section 4.4 Revised Power up Sequence Page 22 Section 4.5 Add build in CGROM ROM D	July 3, 2014

Contents

1. Basic Specifications

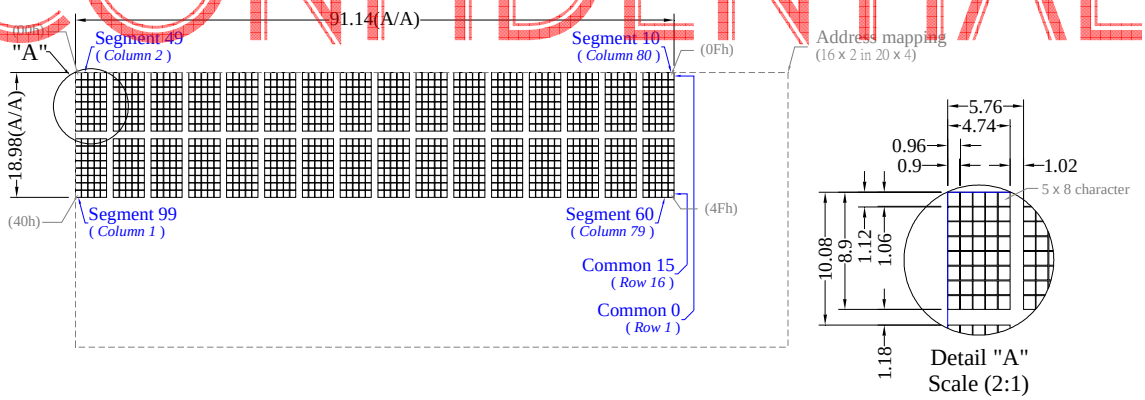
1.1 Display Specifications

1) Display Mode : Passive Matrix
2) Display Color : Monochrome (White)
3) Drive Duty : 1/16 Duty

1.2 Mechanical Specifications

1) Outline Drawing : According to the annexed outline drawing
2) Number of Characters : 16 Characters (5 × 8) × 2 Lines
3) Module Size : 141.80 × 26.50 × 2.00 (mm)
4) Panel Size : 105.00 × 26.50 × 2.00 (mm) including "Anti-Glare" Polarizer
5) Active Area : 91.14 × 18.98 (mm)
6) Character Pitch : 5.76 × 10.08 (mm)
7) Character Size : 4.74 × 8.90 (mm)
8) Pixel Pitch : 0.96 × 1.12 (mm)
9) Pixel Size : 0.90 × 1.06 (mm)
10) Weight : 11.5 (g) ± 10%

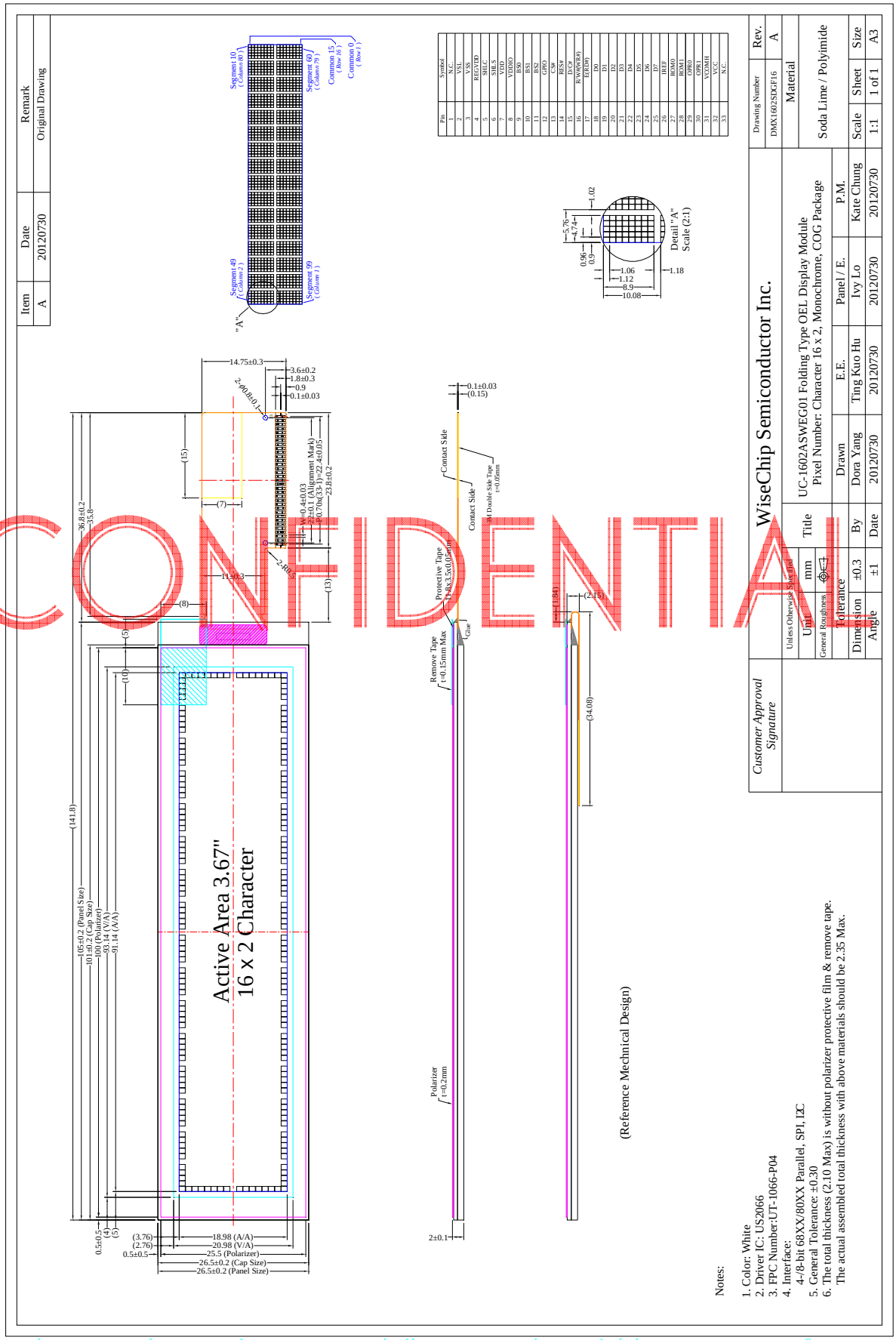
1.3 Active Area / Address Mapping & Character Construction



Address Mapping

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Line 1	00h	01h	02h	03h	04h	05h	06h	07h	08h	09h	0Ah	0Bh	0Ch	0Dh	0Eh	0Fh
Line 2	40h	41h	42h	43h	44h	45h	46h	47h	48h	49h	4Ah	4Bh	4Ch	4Dh	4Eh	4Fh

1.4 Mechanical Drawing



1.5 Pin Definition

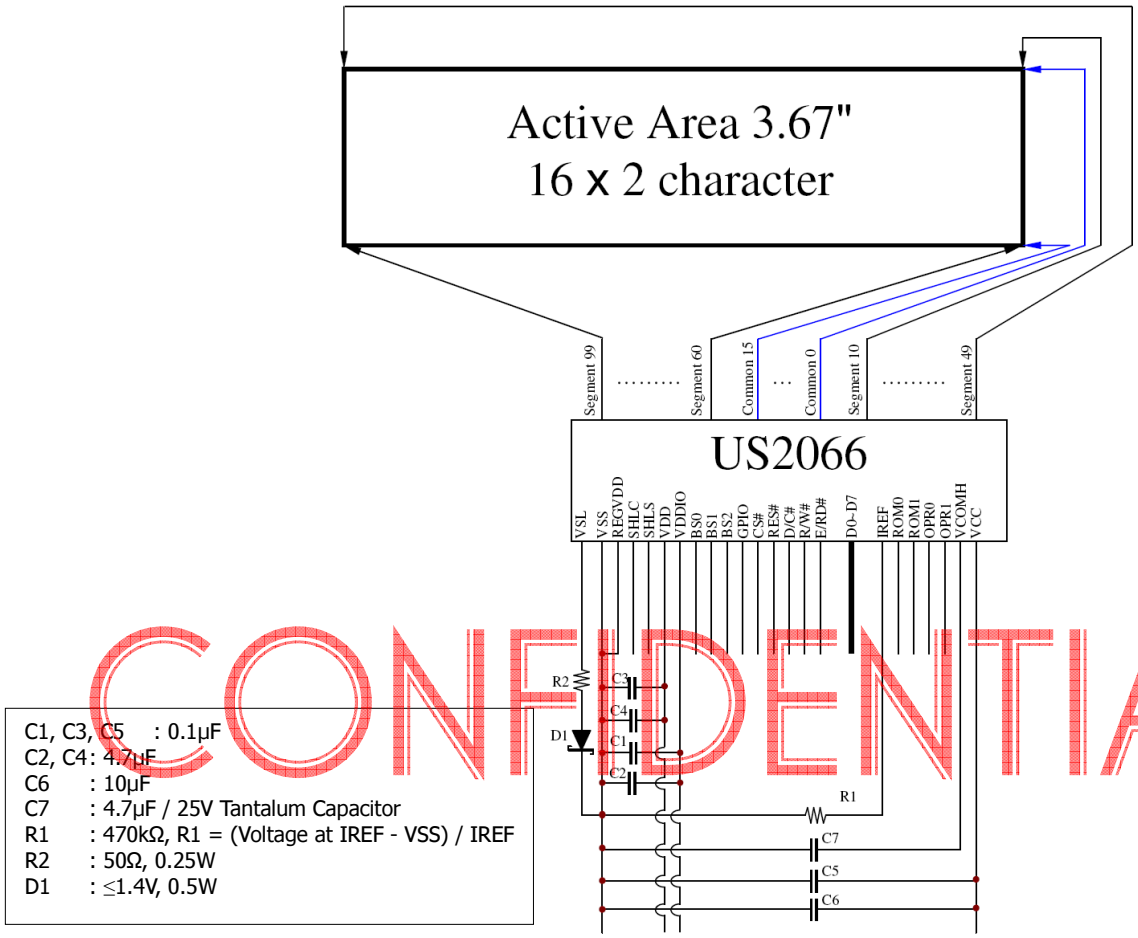
Pin Number	Symbol	I/O	Function
Power Supply			
7	VDD	P	**Power Supply for Logic Circuit** This is a voltage supply pin which is supplied externally or regulated internally. A capacitor should be connected between this pin and V_{SS} under all circumstances. When internal V_{DD} is disabled, this is a power input pin. It must be connected to V_{DDIO} or external source and always be equal to or lower than V_{DDIO}. (Low Voltage I/O Application) When internal V_{DD} is enabled, it is regulated internally from V_{DDIO}. (*5V I/O Application*)
8	VDDIO	P	**Power Supply for Interface Logic Level** This is a voltage supply pin. It should match with the MCU interface voltage level and must be connected to external source
3	VSS	P	**Ground of OEL System** This is a ground pin. It also acts as a reference for the logic pins, the OEL driving voltages, and the analog circuits. It must be connected to external ground.
32	VCC	P	**Power Supply for OEL Panel** This is the most positive voltage supply pin of the chip. It must be connected to external source.
Driver			
26	IREF	I	**Current Reference for Brightness Adjustment** This pin is segment current reference pin. A resistor should be connected between this pin and V_{SS}. Set the current at 15μA.
31	VCOMH	P	**Voltage Output High Level for COM Signal** This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and V_{SS}.
2	VSL	P	**Voltage Output Low Level for SEG Signal** This is segment voltage reference pin. When external V_{SL} is not used, this pin should be left open. When external V_{SL} is used, this pin should connect with resistor and diode to ground.
External IC Communication			
12	GPIO	I/O	**General Purpose Input/Output** This pin could be left open individually or have signal inputted/outputted. It is able to use as the external DC/DC converter circuit enabled/disabled control or other applications.
Configuration			
4	REGVDD	I	**5V I/O Regulator Configuration** This is internal V_{DD} regulator selection pin in 5V I/O application mode. When this pin is pulled "Low", internal V_{DD} regulator is disabled. (Low Voltage I/O Application) When this pin is pulled "High", internal V_{DD} regulator is enabled. (*5V I/O Application*)
5	SHLC	I	**Scanning Direction for COM Signal** This pin is used to determine COM output scanning direction. It can still be programmable and defined by fundamental command.
6	SHLS	I	**Mapping Direction for SEG Signal** This pin is used to change the mapping between the display data column address and the segment driver. It can still be programmable and defined by fundamental command.
27 28	ROM0 ROM1	I	**Built-in Character ROM Selection** These pins are used to select the appropriate character ROM. See the following table & Section 4.5: ROM A (Page 19): ROM0 = 0, ROM1 = 0 ROM B (Page 20): ROM0 = 1, ROM1 = 0 ROM C (Page 21): ROM0 = 0, ROM1 = 1 S/W selectable: ROM0 = 1, ROM1 = 1 It can still be programmable and defined by extended command.

1.5 Pin Definition (Continued)

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td colspan="4">Configuration (Continued)</td></tr>
<tr><td>29
30</td><td>OPR0
OPR1</td><td>I</td><td>Character ROM/RAM Management
These pins are used to manage the character number of character generator. See the following table & Section 4.6:
<table>
<tr><th>CGROM</th><th>CGRAM</th><th>OPR0</th><th>OPR1</th></tr>
<tr><td>240</td><td>8</td><td>0</td><td>0</td></tr>
<tr><td>248</td><td>8</td><td>1</td><td>0</td></tr>
<tr><td>250</td><td>6</td><td>0</td><td>1</td></tr>
<tr><td>256</td><td>0</td><td>1</td><td>1</td></tr>
</table>
It can still be programmable and defined by extended command.</td></tr>
<tr><td colspan="4">Interface</td></tr>
<tr><td>9
10
11</td><td>BS0
BS1
BS2</td><td>I</td><td>Communicating Protocol Selection
These pins are MCU interface selection input. See the following table:
<table>
<tr><th></th><th>BS0</th><th>BS1</th><th>BS2</th></tr>
<tr><td>I²C</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Serial</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>4-bit 68XX Parallel</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>4-bit 80XX Parallel</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>8-bit 68XX Parallel</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>8-bit 80XX Parallel</td><td>0</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>14</td><td>RES#</td><td>I</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.</td></tr>
<tr><td>13</td><td>CS#</td><td>I</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>15</td><td>D/C#</td><td>I</td><td>Data/Command Control
This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 will be interpreted as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register.
In I²C mode, this pin acts as SA0 for slave address selection.
When serial interface mode is selected, this pin must be connected to V_{SS}.
For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.</td></tr>
<tr><td>17</td><td>E/RD#</td><td>I</td><td>Read/Write Enable or Read
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low.
When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.
When serial or I²C mode is selected, this pin must be connected to V_{SS}.</td></tr>
<tr><td>16</td><td>R/W#</td><td>I</td><td>Read/Write Select or Write
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode.
When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.
When serial or I²C mode is selected, this pin must be connected to V_{SS}.</td></tr>
<tr><td>18~25</td><td>D0~D7</td><td>I/O</td><td>Host Data Input/Output Bus
These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D0 will be the serial clock input SCLK; D1 will be the serial data input SID and D2 will be the serial clock output SOD. When I²C mode is selected, D2, D1 should be tired together and serve as SDA_{OUT}, SDA_{IN} in application and D0 is the serial clock input, SCL.
Unused pins must be connected to V_{SS} except.</td></tr>
<tr><td colspan="4">Reserve</td></tr>
<tr><td>1, 33</td><td>N.C. (GND)</td><td>-</td><td>Reserved Pin (Supporting Pin)
The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.</td></tr>
</table>

1.6 Block Diagram

1.6.1 Low Voltage I/O Application



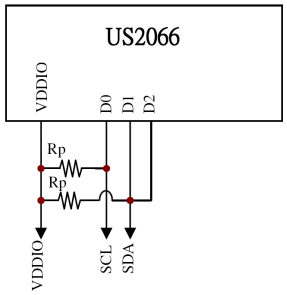
* SHLC, SHLC, ROM0, ROM1, OPR0 and OPR1 should be configured.

MCU Interface Selection : base on BS0, BS1 and BS2 connection
Pins connected to MCU interface : CS#,RES#,D/C#,R/W#,E/RD#, and D0~D7 showed as following table.

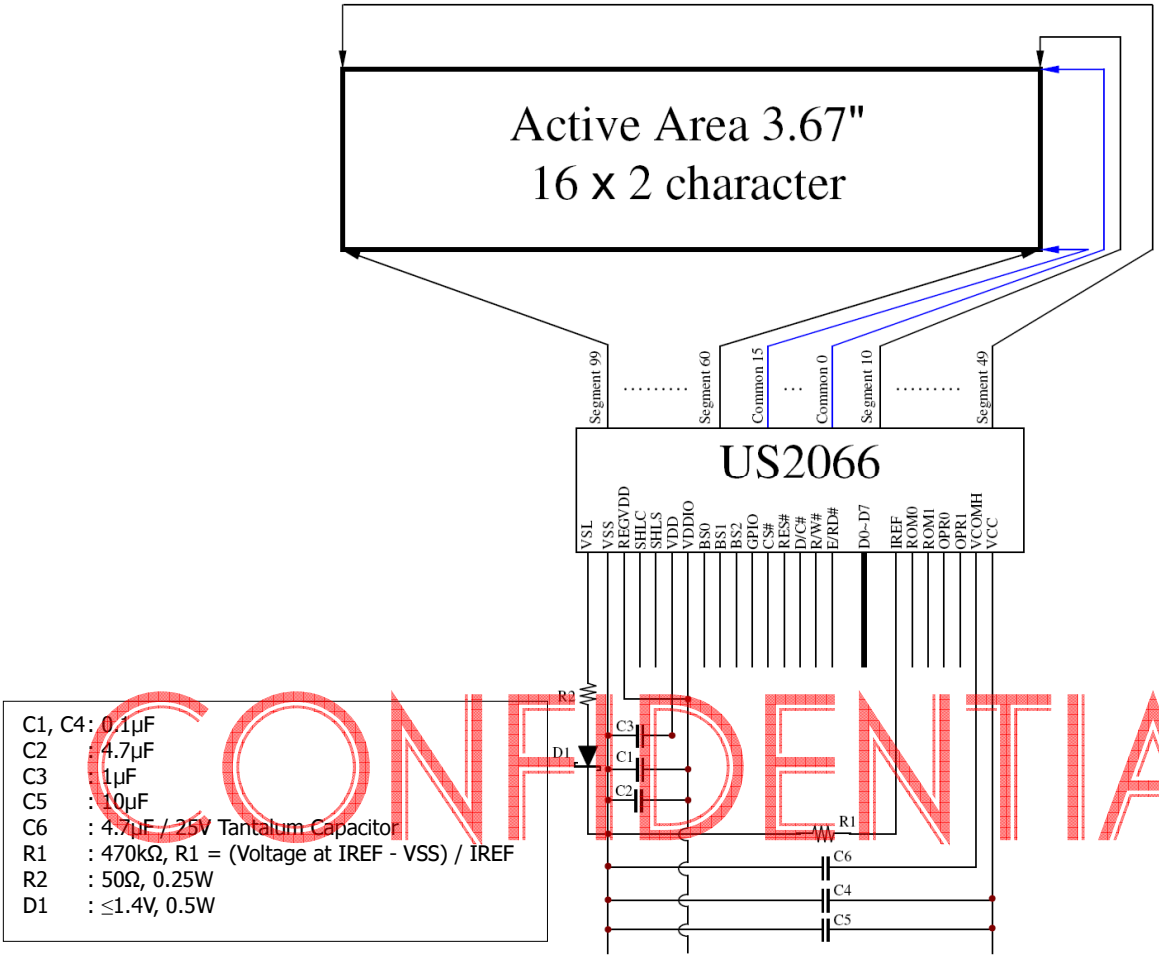
BS2	BS1	BS0	Interface mode	Data bus								Control bus				
				D7	D6	D5	D4	D3	D2	D1	D0	CS#	D/C#	R/W#	E/RD#	RES#
0	0	0	Serial	**0**	**0**	**0**	**0**	**0**	SOD	SID	SCLK	CS#	**0**	**0**	**0**	RES#
0	1	0	I^2C	**0**	**0**	**0**	**0**	**0**	SDA_{OUT}	SDA_{IN}	SCL	**0**	SA0	**0**	**0**	RES#
1	0	0	8-bit 6800	D7	D6	D5	D4	D3	D2	D1	D0	CS#	D/C#	R/W#	E	RES#
1	0	1	4-bit 6800	D7	D6	D5	D4	**0**	**0**	**0**	**0**	CS#	D/C#	R/W#	E	RES#
1	1	0	8-bit 8080	D7	D6	D5	D4	D3	D2	D1	D0	CS#	D/C#	WR#	RD#	RES#
1	1	1	4-bit 8080	D7	D6	D5	D4	**0**	**0**	**0**	**0**	CS#	D/C#	WR#	RD#	RES#

Note :

a. " 0 " is connected to VSS.
b. " 1 " is connected to VDDIO.
c. When I2C mode is selected , SDA and SCL need connected a pull up resistor to VDDIO. Showed as the Fig. .



1.6.2 5V I/O Application

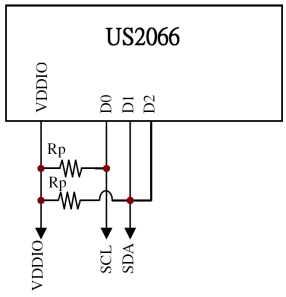


* SHLC, SHLC, ROM0, ROM1, OPR0 and OPR1 should be configured.

MCU Interface Selection : base on BS0, BS1 and BS2 connection
Pins connected to MCU interface : CS#, RES#, D/C#, R/W#, E/RD#, and D0~D7 showed as following table.

BS2	BS1	BS0	Interface mode	Data bus								Control bus				
				D7	D6	D5	D4	D3	D2	D1	D0	CS#	D/C#	R/W#	E/RD#	RES#
0	0	0	Serial	**0**	**0**	**0**	**0**	**0**	SOD	SID	SCLK	CS#	**0**	**0**	**0**	RES#
0	1	0	I^2C	**0**	**0**	**0**	**0**	**0**	SDA_{OUT}	SDA_{IN}	SCL	**0**	SA0	**0**	**0**	RES#
1	0	0	8-bit 6800	D7	D6	D5	D4	D3	D2	D1	D0	CS#	D/C#	R/W#	E	RES#
1	0	1	4-bit 6800	D7	D6	D5	D4	**0**	**0**	**0**	**0**	CS#	D/C#	R/W#	E	RES#
1	1	0	8-bit 8080	D7	D6	D5	D4	D3	D2	D1	D0	CS#	D/C#	WR#	RD#	RES#
1	1	1	4-bit 8080	D7	D6	D5	D4	**0**	**0**	**0**	**0**	CS#	D/C#	WR#	RD#	RES#

Note :
a. ” 0 ” is connected to VSS.
b. ” 1 ” is connected to VDDIO.
c. When I2C mode is selected , SDA and SCL need connected a pull up resistor to VDDIO. Showed as the Fig. .



2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V_{DD}	-0.3	6	V	1, 2
Supply Voltage for I/O Pins	V_{DDIO}	-0.3	6	V	1, 2
Supply Voltage for Display	V_{CC}	0	15	V	1, 2
Operating Temperature	T_{OP}	-40	85	°C	3
Storage Temperature	T_{STG}	-40	90	°C	3
Life Time (100 cd/m^2)		40,000	-	hour	4
Life Time (80 cd/m^2)		55,000	-	hour	4

Note 1: All the above voltages are on the basis of "V_{SS} = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: V_{CC} = 12.0V, T_a = 25°C, 50% Checkerboard.
Software configuration follows Section 4.4 Initialization.
End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

3. Optics & Electrical Characteristics

3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	Note 5	80	100	-	cd/m^2
C.I.E. (White)	(x) (y)	C.I.E. 1931	0.25 0.27	0.29 0.31	0.33 0.35	
Dark Room Contrast	CR		-	>10,000:1	-	
Viewing Angle			-	Free	-	degree

* Optical measurement taken at V_{DDIO} = 2.8V or 5.0V, V_{CC} = 12.0V.
Software configuration follows Section 4.4 Initialization.

3.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}	(Low Voltage I/O Application)	2.4	2.8	V_{DDIO}	V
Supply Voltage for I/O Pins	V_{DDIO}		2.4	2.8	3.6	V
Supply Voltage for Logic	V_{DD}	(5V I/O Application)	-	-	-	V
Supply Voltage for I/O Pins	V_{DDIO}		4.4	5.0	5.5	V
Supply Voltage for Display	V_{CC}	Note 5	11.5	12.0	12.5	V
High Level Input	V_{IH}	I_{OUT} = 100μA, 3.3MHz	0.8×V_{DDIO}	-	V_{DDIO}	V
Low Level Input	V_{IL}	I_{OUT} = 100μA, 3.3MHz	0	-	0.2×V_{DDIO}	V
High Level Output	V_{OH}	I_{OUT} = 100μA, 3.3MHz	0.9×V_{DDIO}	-	V_{DDIO}	V
Low Level Output	V_{OL}	I_{OUT} = 100μA, 3.3MHz	0	-	0.1×V_{DDIO}	V
Operating Current for V_{DD}	I_{DD}		-	180	300	μA
Operating Current for V_{CC}	I_{CC}	Note 6	-	18.0	21.6	mA
		Note 7	-	27.0	32.4	mA
		Note 8	-	46.0	55.2	mA
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$		-	1	10	μA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$		-	2	10	μA

Note 5: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.
Note 6: V_{DDIO} = 2.8V or 5.0V, V_{CC} = 12.0V, 30% Display Area Turn on.
Note 7: V_{DDIO} = 2.8V or 5.0V, V_{CC} = 12.0V, 50% Display Area Turn on.
Note 8: V_{DDIO} = 2.8V or 5.0V, V_{CC} = 12.0V, 100% Display Area Turn on.

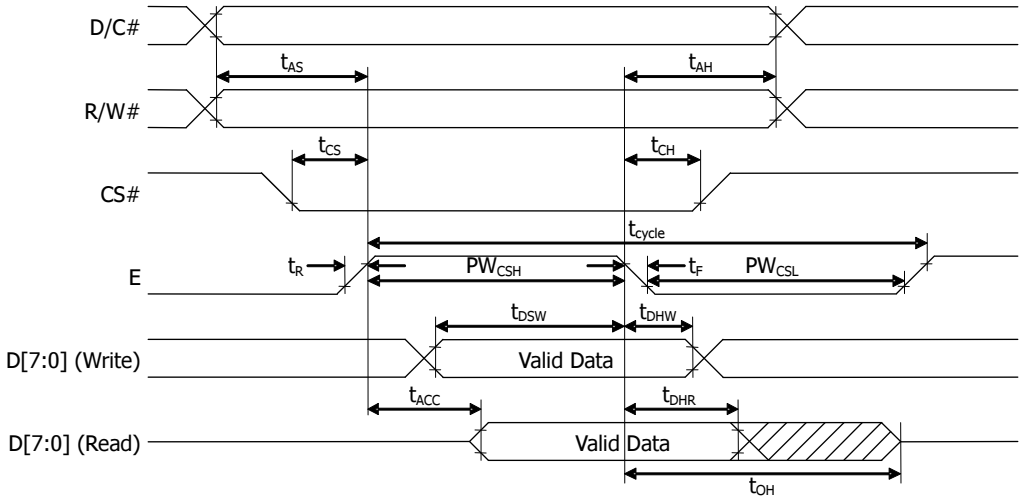
* Software configuration follows Section 4.4 Initialization.

3.3 AC Characteristics

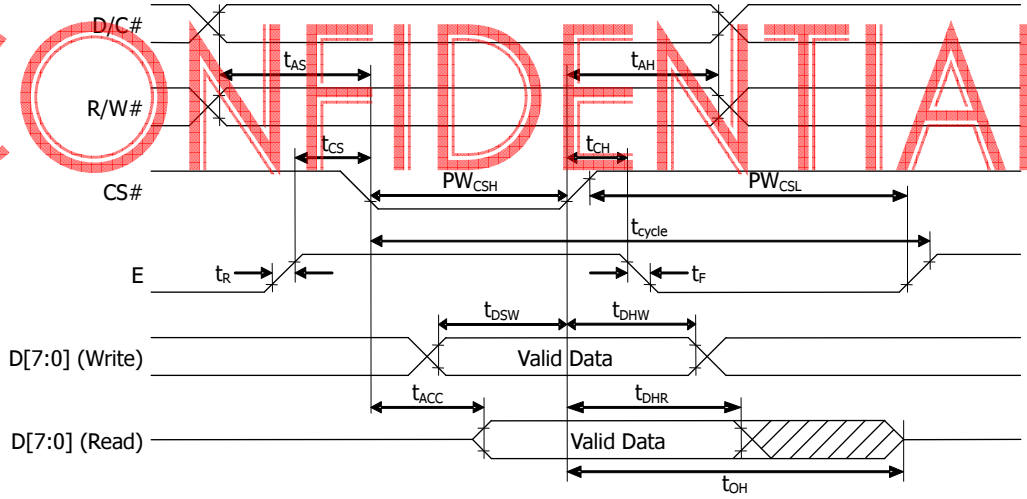
3.3.1 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time (Write Cycle)	400	-	ns
t_{AS}	Address Setup Time	13	-	ns
t_{AH}	Address Hold Time	17	-	ns
t_{DSW}	Write Data Setup Time	35	-	ns
t_{DHW}	Write Data Hold Time	18	-	ns
t_{DHR}	Read Data Hold Time	13	-	ns
t_{OH}	Output Disable Time	-	90	ns
t_{ACC}	Access Time (RAM)	-	200	ns
	Access Time (Command)			
t_{CS}	Chip Select Time	0	-	ns
t_{CH}	Chip Select Hold Time	0	-	ns
PW_{CSL}	Chip Select Low Pulse Width (Read RAM)	250	-	ns
	Chip Select Low Pulse Width (Read Command)	250		
	Chip Select Low Pulse width (Write)	50		
PW_{CSH}	Chip Select High Pulse Width (Read)	155	-	ns
	Chip Select High Pulse Width (Write)	55		
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DDIO} - V_{SS} = 2.4V to 3.6V / 4.4V to 5.5V, T_a = 25°C)



(CS# "Low Pulse Width" > E "High Pulse Width")

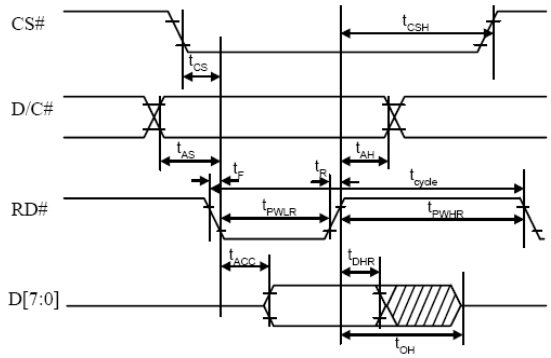


(CS# "Low Pulse Width" < E "High Pulse Width")

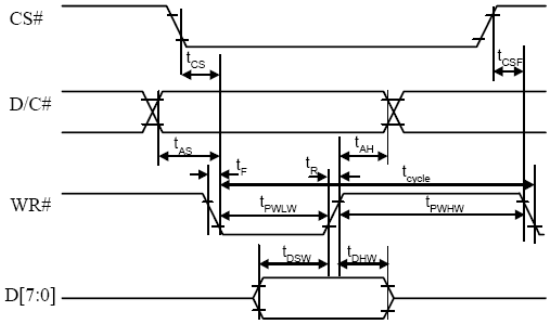
3.3.2 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time (Write Cycle)	400	-	ns
t_{AS}	Address Setup Time	13	-	ns
t_{AH}	Address Hold Time	17	-	ns
t_{DSW}	Write Data Setup Time	35	-	ns
t_{DHW}	Write Data Hold Time	18	-	ns
t_{DHR}	Read Data Hold Time	13	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time (RAM)	-	200	ns
	Access Time (Command)			
t_{CS}	Chip Select Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	0	-	ns
PW_{CSL}	Chip Select Low Pulse Width (Read RAM) - t_{PWLR}	250	-	ns
	Chip Select Low Pulse Width (Read Command) - t_{PWLR}	250		
	Chip Select Low Pulse width (Write) - t_{PWLW}	50		
PW_{CSH}	Chip Select High Pulse Width (Read) - t_{PWHR}	155	-	ns
	Chip Select High Pulse Width (Write) - t_{PWHW}	55		
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DDIO} - V_{SS} = 2.4V to 3.6V / 4.4V to 5.5V, T_a = 25°C)



(***Read Timing***)

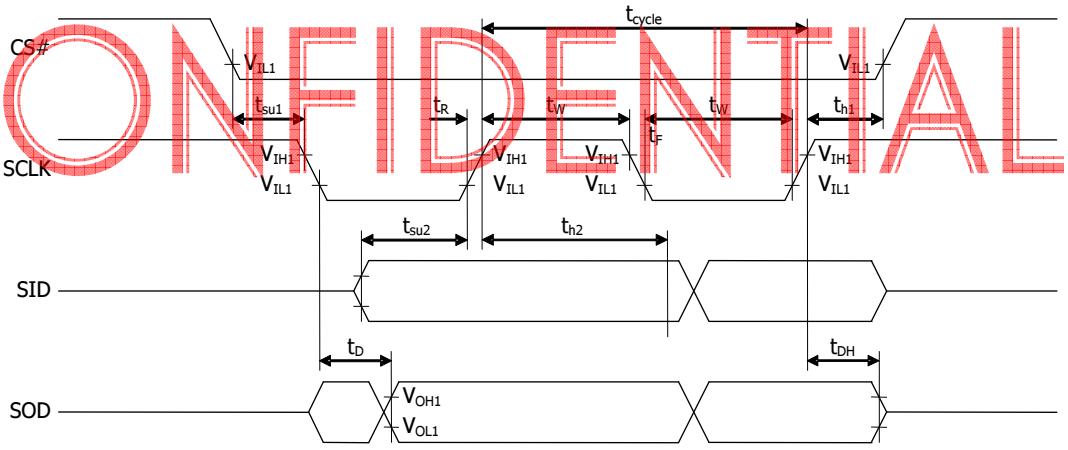


(***Write Timing***)

3.3.3 Serial Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Serial Clock Cycle Time	1	20	μs
t_{su1}	Chip Select Setup Time	60	-	ns
t_{h1}	Chip Select Hold Time	20	-	ns
t_{su2}	Serial Input Data Setup Time	200	-	ns
t_{h2}	Serial Input Data Hold Time	20	-	ns
t_D	Serial Output Data Delay Time	200	-	ns
t_{DH}	Serial Output Data Hold Time	10	-	ns
t_W	Serial Clock Width (Low, High)	400	-	ns
t_R	Serial Clock Rise Time	-	15	ns
t_F	Serial Clock Fall Time	-	15	ns

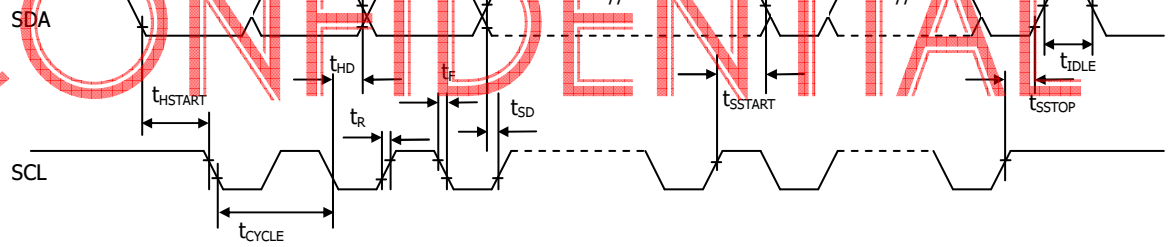
* (V_{DDIO} - V_{SS} = 2.4V to 3.6V / 4.4V to 5.5V, T_a = 25°C)



3.3.4 I^2C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	μs
t_{HSTART}	Start Condition Hold Time	0.6	-	μs
t_{HD}	Data Hold Time (for "SDA_{OUT}" Pin)	5	-	ns
	Data Hold Time (for "SDA_{IN}" Pin)	460		
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	μs
t_{SSTOP}	Stop Condition Setup Time	0.6	-	μs
t_R	Rise Time for Data and Clock Pin		300	ns
t_F	Fall Time for Data and Clock Pin		300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3	-	μs

* (V_{DDIO} - V_{SS} = 2.4V to 3.6V / 4.4V to 5.5V, T_a = 25°C)



4. Functional Specification

4.1 Commands

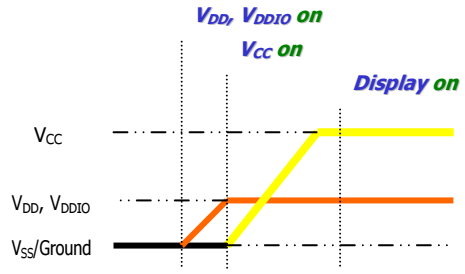
Refer to the Technical Manual for the US2066

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

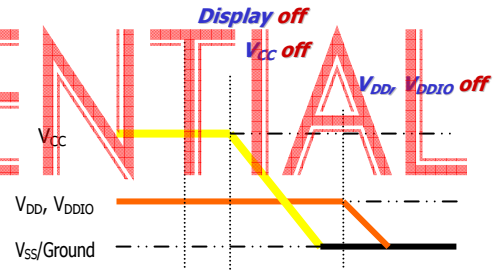
4.2.1 Power up Sequence:

1. Power up V_{DD} & V_{DDIO}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
   (When V_{CC} is stable)
7. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
   (When V_{CC} is reach 0 and panel is completely discharges)
4. Power down V_{DD} & V_{DDIO}



Note 9:

1) Since an ESD protection circuit is connected between V_{DD}, V_{DDIO} and V_{CC} inside the driver IC, V_{CC} becomes lower than V_{DD} & V_{DDIO} whenever V_{DD} & V_{DDIO} is ON and V_{CC} is OFF.
2) V_{CC} should be kept float (disable) when it is OFF.
3) Power Pins (V_{DD}, V_{DDIO}, V_{CC}) can never be pulled to ground under any circumstance.
4) V_{DD} & V_{DDIO} should not be power down before V_{CC} power down.

4.3 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

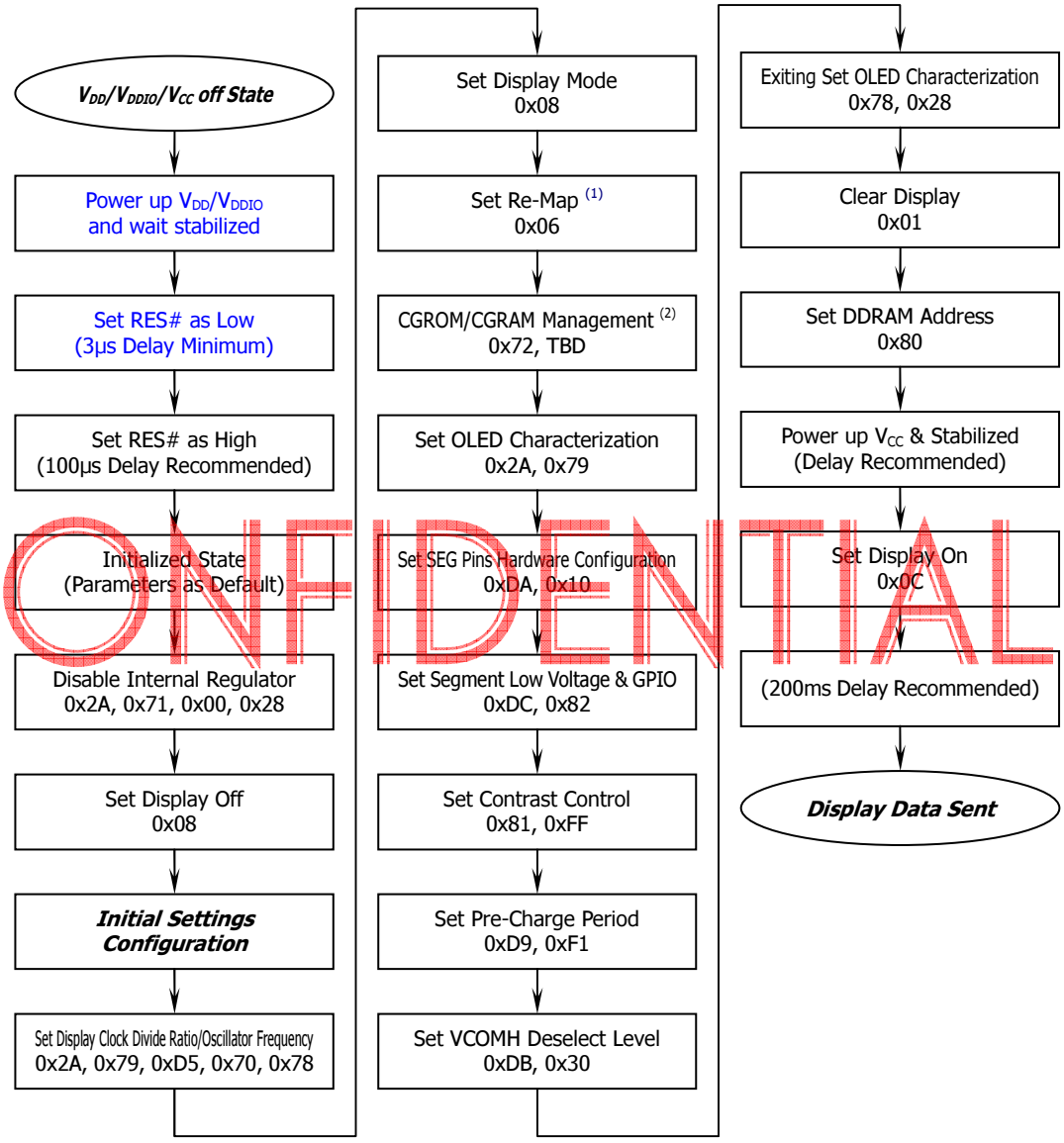
1. Display is OFF
2. 5×8 Character Mode
3. Display start position is set at display RAM address 0
4. CGRAM address counter is set at 0
5. Cursor is OFF
6. Blink is OFF
7. Contrast control register is set at 7Fh
8. OLED command set is disabled

4.4 Actual Application Example

Command usage and explanation of an actual example

4.4.1 Low Voltage I/O Application

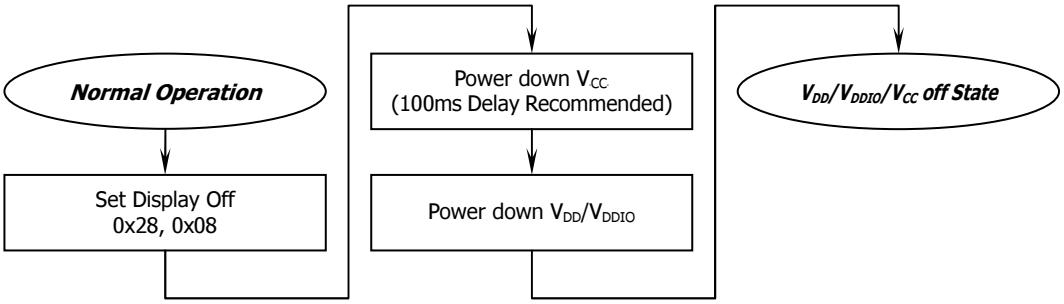
<Power up Sequence>



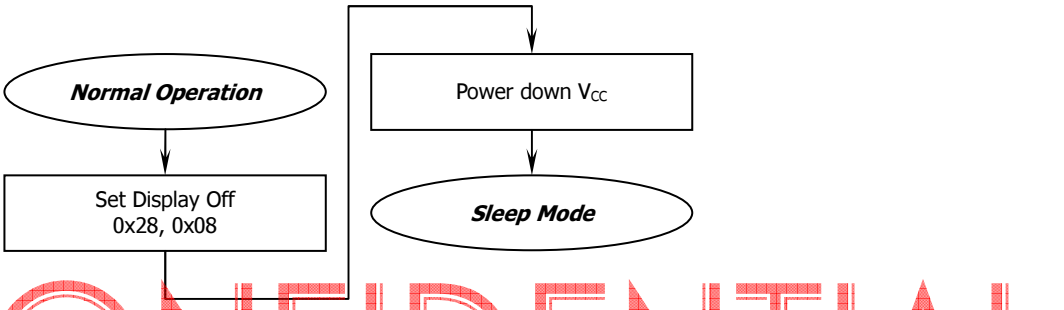
(1) This command could be programmable or defined by pin configuration.
(2) This command could be programmable or defined by pin configuration. The written value of the parameter should depend on the selection from Section 4.5 & 4.6

If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

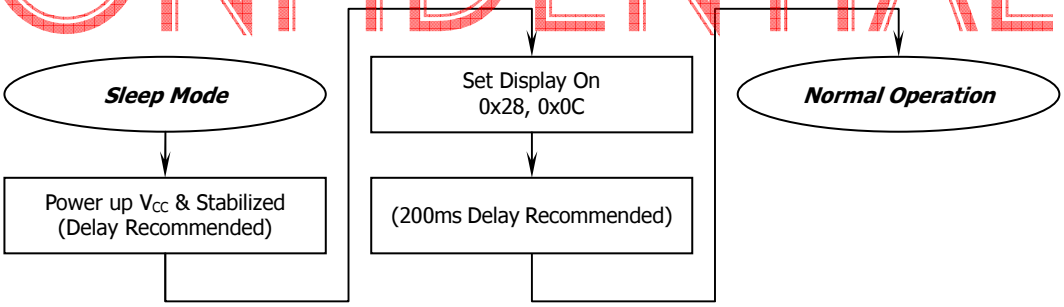
<Power down Sequence>



<Entering Sleep Mode>

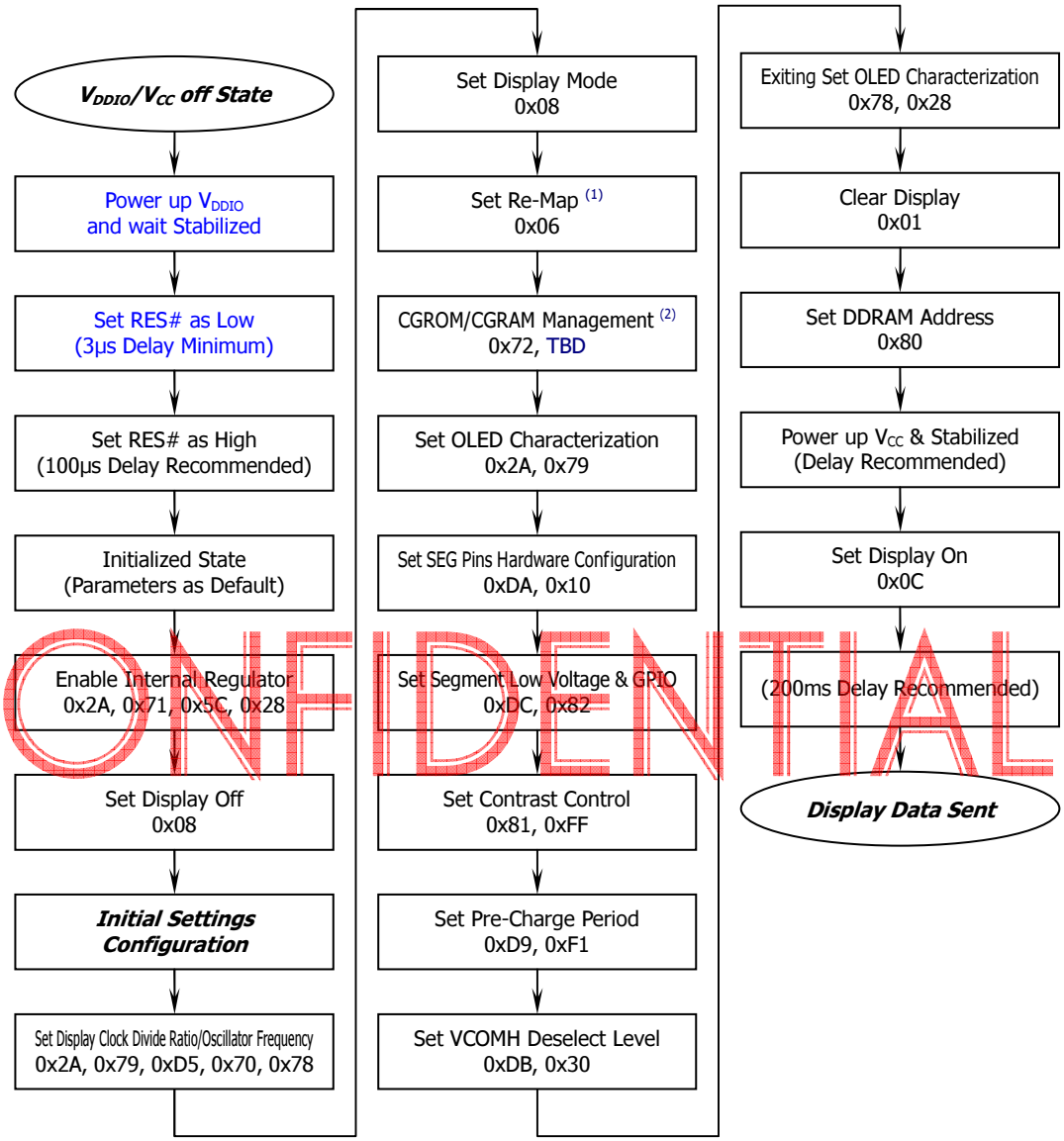


<Exiting Sleep Mode>



4.4.2 5V I/O Application

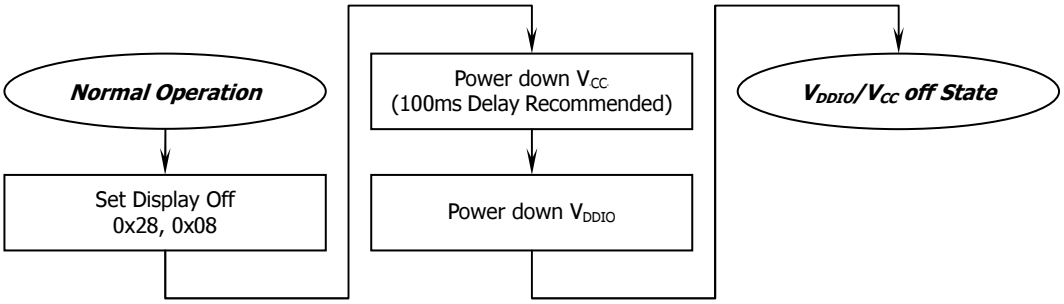
<Power up Sequence>



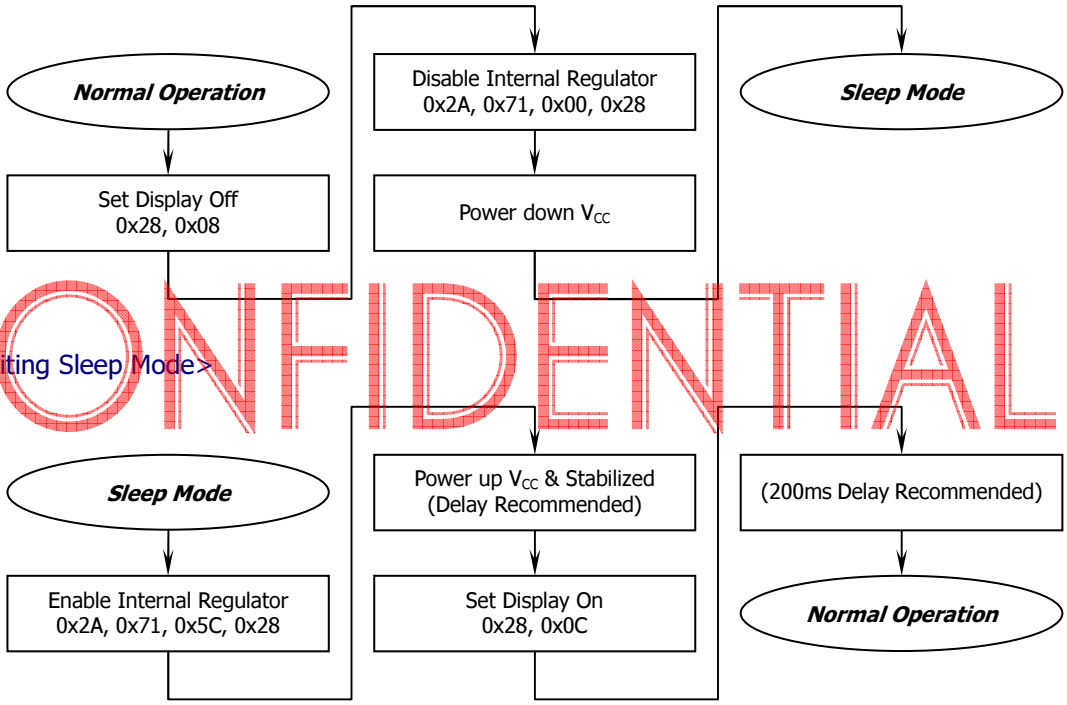
(1) This command could be programmable or defined by pin configuration.
(2) This command could be programmable or defined by pin configuration. The written value of the parameter should depend on the selection from Section 4.5 & 4.6

If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

<Power down Sequence>



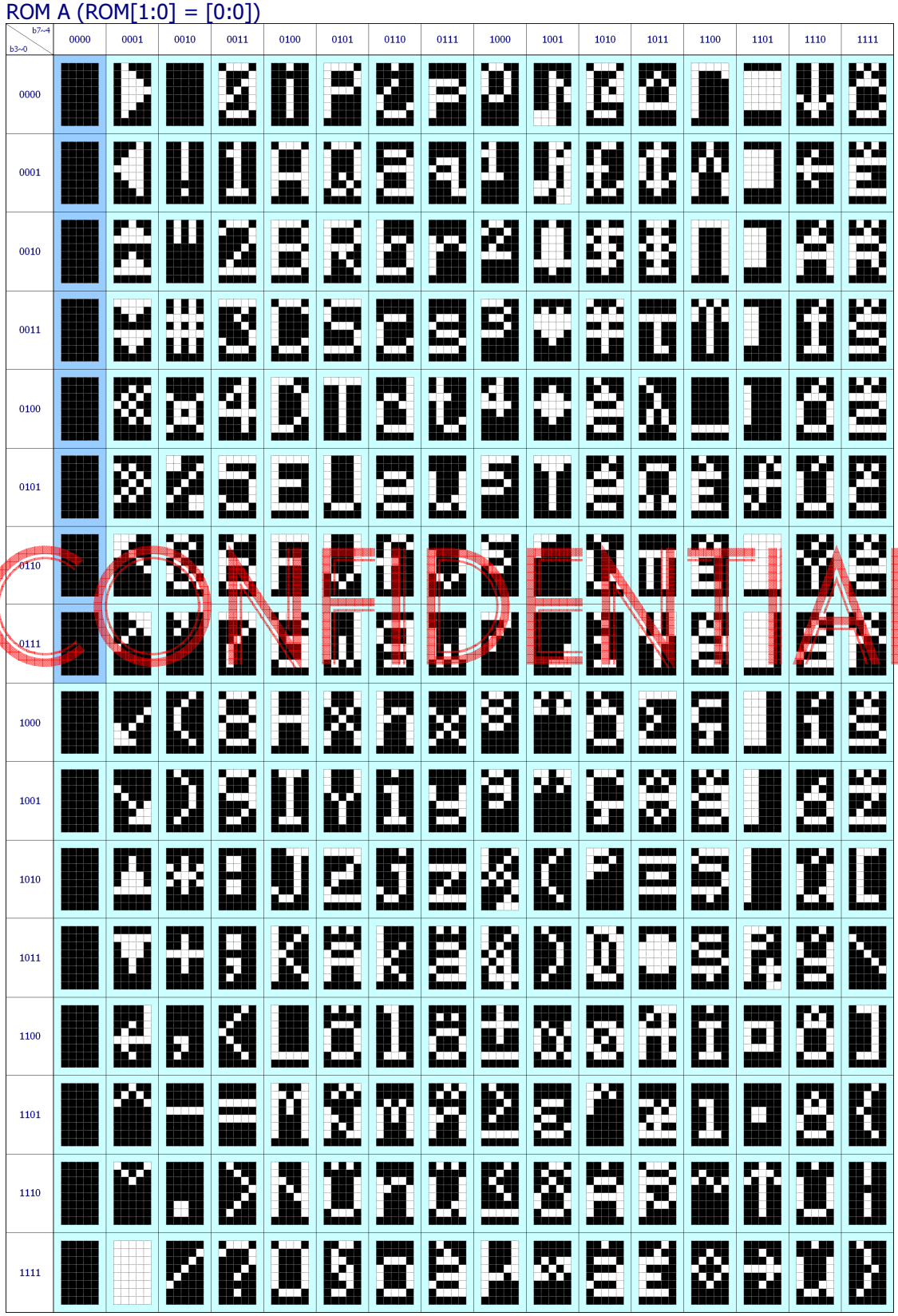
<Entering Sleep Mode>



<Exiting Sleep Mode>

4.5 Built-in CGROM (Character Generator ROM)

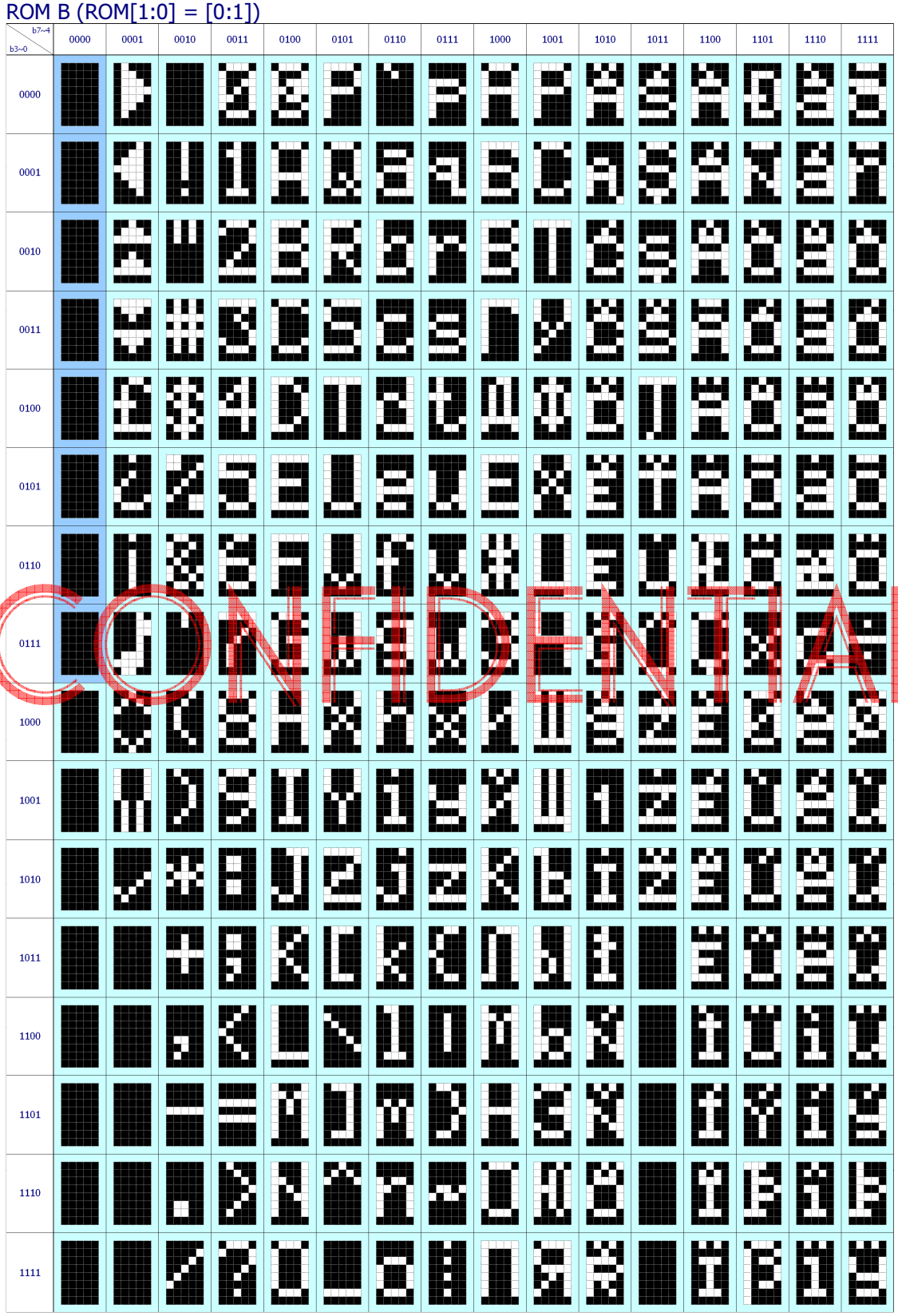
ROM A (ROM[1:0] = [0:0])



Language: English, Irish, Spanish, Dutch (2), Danish, Norwegian, Swedish, Finnish, Czech (7), Slovene, Hungarian (2), Turkish (1)

The number in the parentheses is showing how many letters might be needed to build and define additionally at CGRAM. The darker background is showing the maximum addresses (00h~07h) those could be allocated by OPR[1:0] setting.

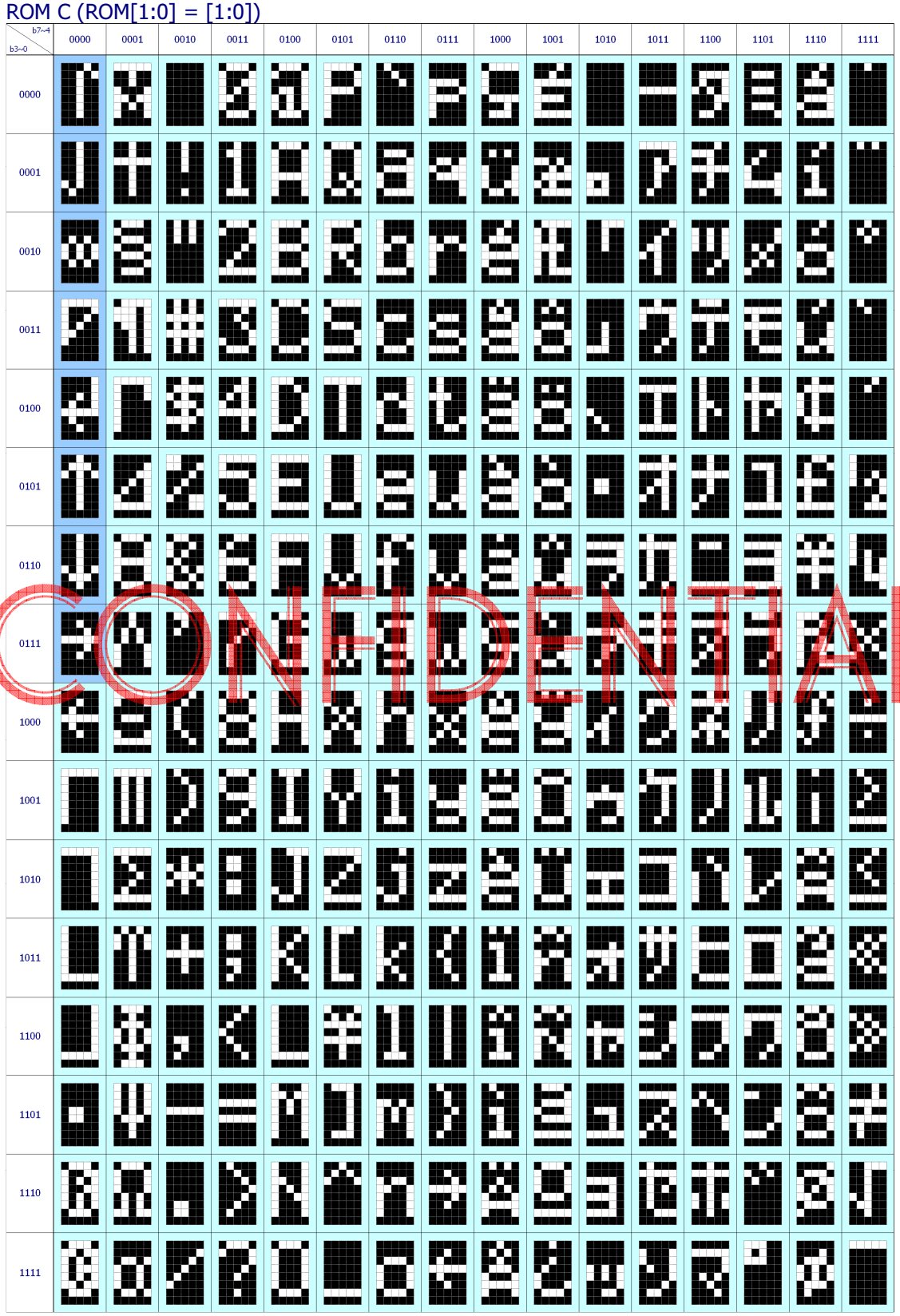
ROM B (ROM[1:0] = [0:1])



Language: English, Irish, Portuguese, Spanish, French (1), Italian, German, Dutch (2), Icelandic, Danish, Norwegian, Swedish, Polish (8), Czech (8), Hungarian (2), Romanian (5), Turkish, Vietnamese (6), Russian (Small Letters)

The number in the parentheses is showing how many letters might be needed to build and define additionally at CGRAM. The darker background is showing the maximum addresses (00h~07h) those could be allocated by OPR[1:0] setting.

ROM C (ROM[1:0] = [1:0])



Language: English, Dutch (2), Japanese, Greek (Small Letters)
The number in the parentheses is showing how many letters might be needed to build and define additionally at CGRAM. The darker background is showing the maximum addresses (00h~07h) those could be allocated by OPR[1:0] setting.

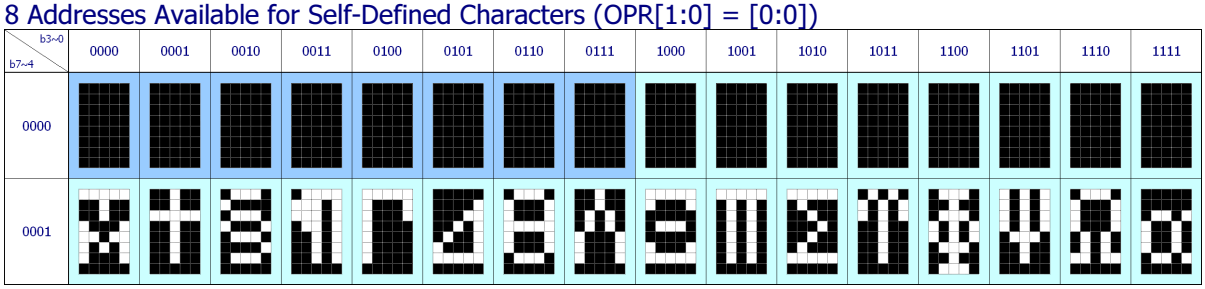
ROM D (ROM[1:0] = [1:1])

Language: English, Dutch (1), Greek, Russian, Belorussian, Ukrainian, Serbian (10), Macedonian (10), Bulgarian, Kazakh (12), Mongolian

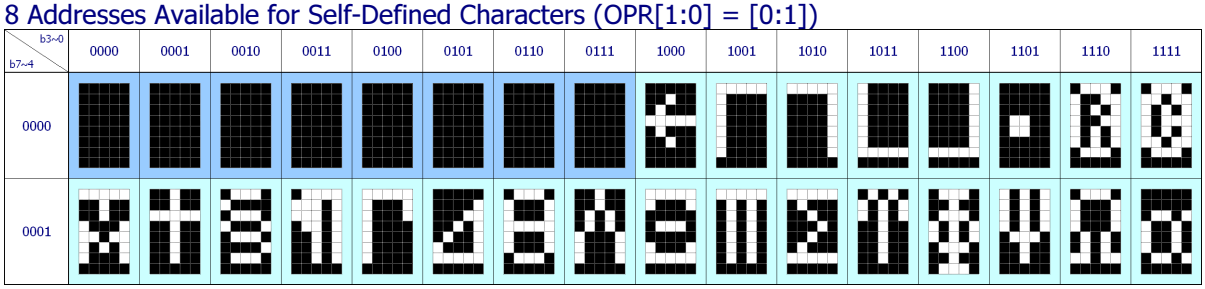
The number in the parentheses is showing how many letters might be needed to build and define additionally at CGRAM. The darker background is showing the maximum addresses (00h~07h) those could be allocated by OPR[1:0] setting.

4.6 Self-Defined CGRAM (Character Generator RAM)

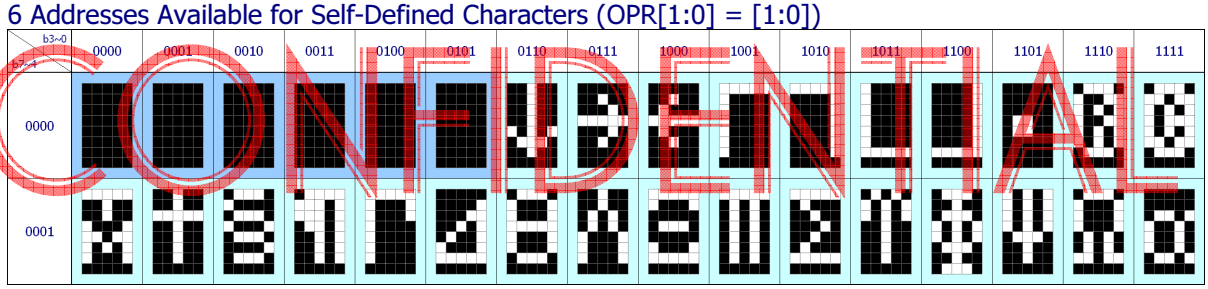
8 Addresses Available for Self-Defined Characters (OPR[1:0] = [0:0])



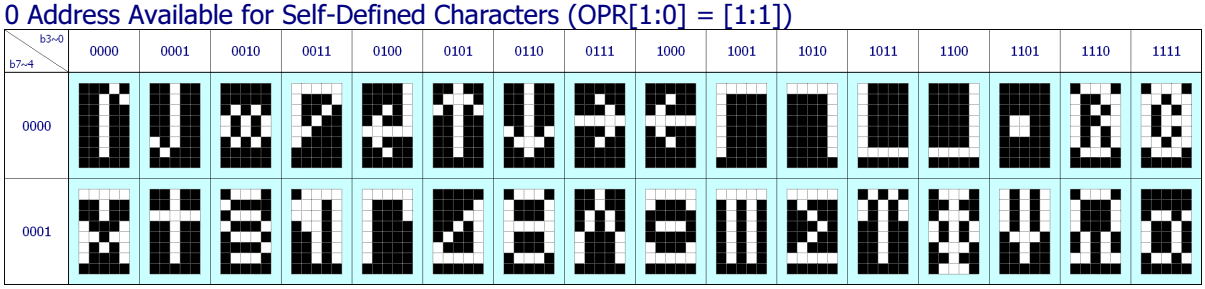
8 Addresses Available for Self-Defined Characters (OPR[1:0] = [0:1])



6 Addresses Available for Self-Defined Characters (OPR[1:0] = [1:0])



0 Address Available for Self-Defined Characters (OPR[1:0] = [1:1])



5. Reliability

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	85°C, 240 hrs	The operational functions work.
Low Temperature Operation	-40°C, 240 hrs	
High Temperature Storage	90°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 240 hrs	
Thermal Shock	-40°C ⇔ 85°C, 100 cycles 60 mins dwell	

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

5.2 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

6. Outgoing Quality Control Specifications

6.1 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	23 ± 5°C
Humidity:	55 ± 15% RH
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	≥ 50cm
Distance between the Panel & Eyes of the Inspector:	≥ 30cm

Finger glove (or finger cover) must be worn by the inspector.
Inspection table or jig must be anti-electrostatic.

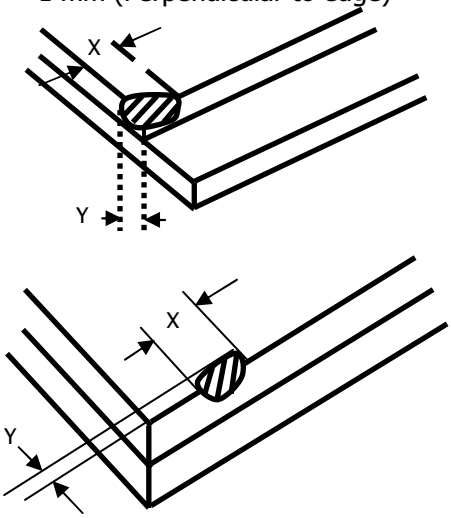
6.2 Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

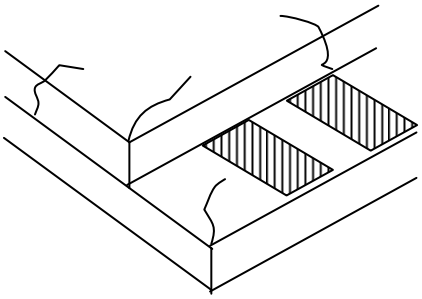
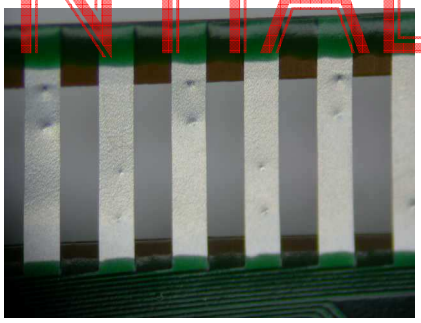
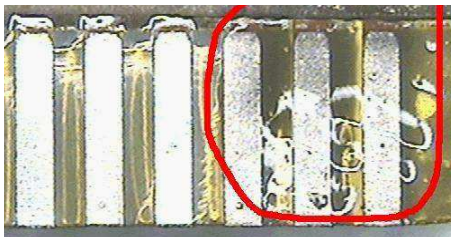
6.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

6.3.1 Cosmetic Check (Display Off) in Non-Active Area

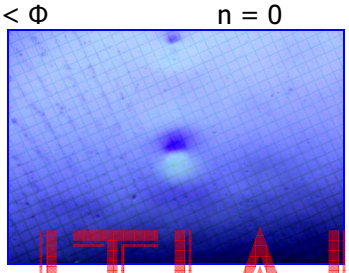
Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge) 

6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Copper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Prober Mark	Acceptable	
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

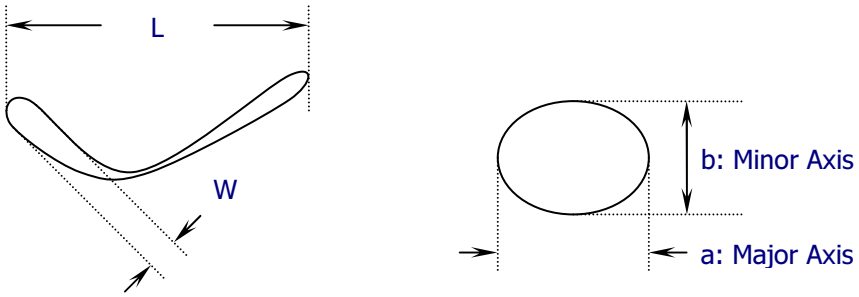
6.3.2 Cosmetic Check (Display Off) in Active Area

It is recommended to execute in clear room environment (class 10k) if actual in necessary.

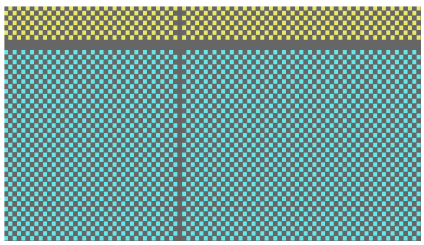
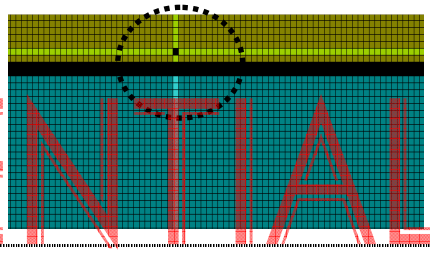
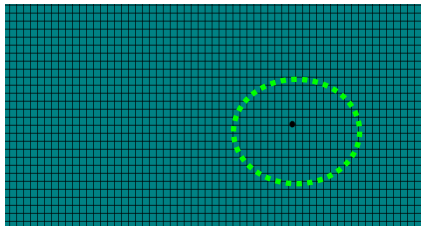
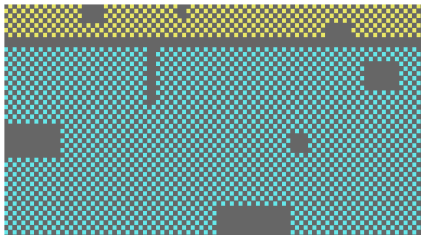
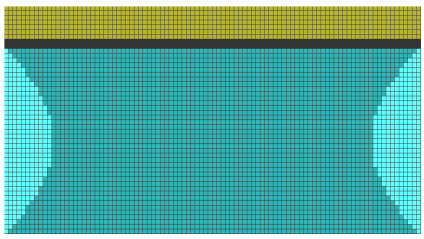
Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	W ≤ 0.1 Ignore W > 0.1 L ≤ 2 n ≤ 1 L > 2 n = 0
Dirt, Black Spot, Foreign Material, (On Polarizer)	Minor	Φ ≤ 0.1 Ignore 0.1 < Φ ≤ 0.25 n ≤ 1 0.25 < Φ n = 0
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	Φ ≤ 0.5 ➔ Ignore if no Influence on Display 0.5 < Φ n = 0 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

* Protective film should not be tear off when cosmetic check.

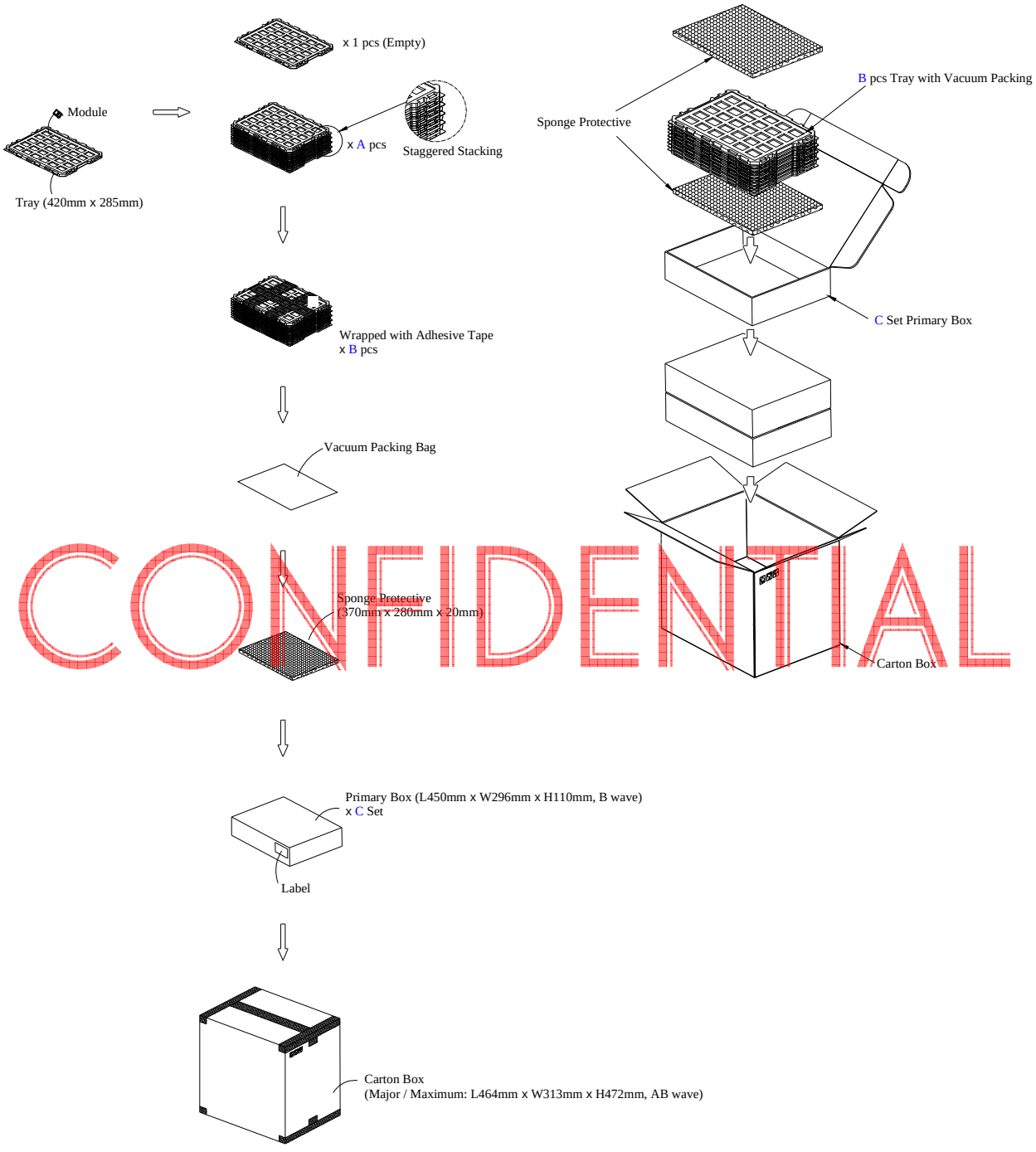
** Definition of W & L & Φ (Unit: mm): Φ = (a + b) / 2



6.3.3 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	

7. Package Specifications



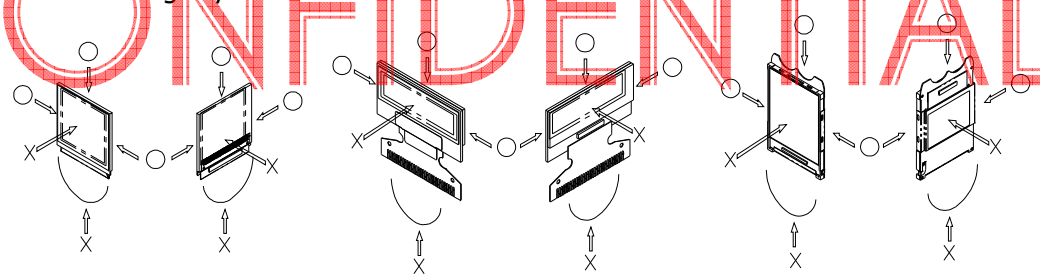
Item		Quantity	
Module		**240**	**per Primary Box**
Holding Trays	**(A)**	**20**	**per Primary Box**
Total Trays	**(B)**	**21**	**per Primary Box (Including 1 Empty Tray)**
Primary Box	**(C)**	**1~4**	**per Carton (4 as Major / Maximum)**

8. Precautions When Using These OEL Display Modules

8.1 Handling Precautions

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
5) When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent

   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.
   Also, pay attention that the following liquid and solvent may spoil the polarizer:
   * Water
   * Ketone
   * Aromatic Solvents
6) Hold OEL display module very carefully when placing OEL display module into the system housing. Do not apply excessive stress or pressure to OEL display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



7) Do not apply stress to the driver IC and the surrounding molded sections.
8) Do not disassemble nor modify the OEL display module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OEL display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
    * Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.
11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

8.2 Storage Precautions

1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps. and, also, avoiding high temperature and high

humidity environment or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from WiseChip Semiconductor Inc.)
At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.

2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

8.3 Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the V_{IL} and V_{IH} specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (V_{DD}). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the OEL display module, fasten the external plastic housing section.
7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
8) The electric potential to be connected to the rear face of the IC chip should be as follows: US2066
   * Connection (contact) to any other potential than the above may lead to rupture of the IC.

8.4 Precautions when disposing of the OEL display modules

1) Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

8.5 Other Precautions

1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.
   Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
   * Pins and electrodes
   * Pattern layouts such as the FPC
3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.
4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
5) We recommend you to construct its software to make periodical refreshment of the operation

statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

Warranty:

The warranty period shall last twelve (12) months from the date of delivery. Buyer shall be completed to assemble all the processes within the effective twelve (12) months. WiseChip Semiconductor Inc. shall be liable for replacing any products which contain defective material or process which do not conform to the product specification, applicable drawings and specifications during the warranty period. All products must be preserved, handled and appearance to permit efficient handling during warranty period. The warranty coverage would be exclusive while the returned goods are out of the terms above.

Notice:

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